Reduction of Cross-talk Noise in VLSI Circuits

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RELATED APPLICATIONS

[0001] This application claims a priority benefit of U.S. Patent Application 60/461,959, filed April 9, 2003, the contents of which are herein incorporated by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] The present invention relates to very large scale integration ("VLSI") circuits and, more particularly, to reducing cross-talk noise in VLSI circuits.

2. Description of the Related Arts

[0003] Conventionally, an integrated circuit chip is comprised of a thin, flat semiconductor substrate having a predefined shape (e.g., rectangular or square) and size (e.g., about 10 millimeters ("mm") to 25 mm on a side). Integrated into one surface of that substrate are a huge number of microscopic transistors. On top of those transistors are several patterned layers of conductive material and several patterned layers of insulating material that are fabricated in a stack. These insulating layers and conductive layers alternate such that an insulating layer separates any two conductive layers.

[0004] All of the conductive layers are patterned to form signal lines that interconnect the transistors, and they are also patterned to form DC voltage busses and ground busses by which power is supplied to the transistors. Some of the signal lines interconnect the

transistors into multiple logic gates, for example logic AND gates, OR gates, NAND gates, and the like. The remaining signal lines interconnect the logic gates to each other so that they may perform some predetermined logic function.

[0005] With present day technology, the typical number of transistors on a single chip is rapidly approaching one billion. Moreover, the number of logic gates that are formed by the transistors is reaching one million, combinations of which are interconnected through appropriate signal lines. Each such interconnection from the output from one logic gate (the driver) to the input of one or more other logic gates (the receivers) is herein called a "net."

[0006] Ideally, the digital signals which are generated by a driver logic gate on one particular net will not affect the digital signals which are generated by any other driver logic gate on any other net. However, whenever two nets have signal line segments that lie next to each other, then a distributed parasitic capacitance will exist between them; and consequently, a voltage transition on one signal line. This is often referred to as an aggressor net and it will cause a certain amount of cross-talk noise (e.g., noise voltage) to be coupled into the other signal line, which is often referred to as a victim net.

[0007] As minimum feature size in circuits is shrinking, signal integrity issues gain importance due to increased coupling between nets in VLSI circuits. This coupling that may result in cross-talk noise (i.e, where the signal on one net (the victim net), is affected by the changes in the signal of its neighboring nets (the aggressor nets)) that can cause functional errors or increase power usage due to spurious switching on victim nets, even though false values are not latched at registers. Decreasing feature sizes affects the cross-talk noise

problem in two ways. First, it increases coupling capacitance between nets. Second, smaller transistors cause faster slew rates.

[0008] Cross-talk noise depends on the amount of coupling capacitance between a victim net and its neighboring nets versus the victim net's capacitance to ground, aggressor net slew rates, and victim net resistance path to power or ground supply. As coupling capacitance to ground capacitance ratio increases, cross-talk noise increases. Similarly, as aggressor slew rates get faster, cross-talk noise increases. Decreasing victim resistance to power or ground supply will decrease cross-talk noise.

[0009] To resolve cross-talk glitch problems, currently different methods are used. Buffering victim nets decreases resistance along discharge path to reduce noise height as well as increasing pin capacitance, which adds capacitance to ground. But this may also make a victim an aggressor, making convergence difficult. Spacing wires apart decreases coupling capacitance, and in effect reduces noise height. However, the effectiveness of this technique is limited in congested designs where introducing extra spacing between wires is not possible.

[0010] Therefore, there is a need for a solution to reduce cross-talk noise in VLSI circuits, while limiting or avoiding disturbance of overall circuit design, while minimizing a number of wires touched and allowing or guaranteeing convergence.

SUMMARY OF THE INVENTION

[0011] The present invention includes a system and a technique to reduce cross-talk noise that comprises increasing the non-coupling capacitance as a percentage of the total

capacitance. In one embodiment the present invention analyzes a circuit configuration to add extra pin capacitance to victim nets to decrease coupling capacitance to ground capacitance ratio. As an example, once cross-talk noise victim nets are identified, extra pin capacitance is added to these nets using a logic library cell, for example, an inverter. Alternatively, any other library element input pin or special capacitance cells may also be used.

[0012] It is noted that in one embodiment, the size of the cell or cells to be added is chosen to add sufficient capacitance to resolve the cross-talk noise problem on a particular net. For example, the extra pin capacitance can be added by connecting an input pin of the correct size inverter or capacitance cell to the victim net. The new cell may be coupled directly with the victim net or it may be placed close to the victim net and connected to the net using incremental routing.

[0013] The present invention includes a number of benefits. For example, the present invention beneficially does not disturb an overall solution for a circuit layout. In addition, the present invention advantageously touches a minimal number of wires, while guaranteeing convergence because new slews are always larger than previous slews.

[0014] The features and advantages described in the specification are not all inclusive and, in particular, many additional features and advantages will be apparent to one of ordinary skill in the art in view of the drawings, specification, and claims. Moreover, it should be noted that the language used in the specification has been principally selected for readability and instructional purposes, and may not have been selected to delineate or circumscribe the inventive subject matter.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The invention has other advantages and features which will be more readily apparent from the following detailed description of the invention and the appended claims, when taken in conjunction with the accompanying drawings, in which:

[0016] Figure 1 illustrates a flow diagram of a process for reducing cross-talk noise between a victim net and one or more aggressor nets in accordance with one embodiment of the present invention.

[0017] Figures 2a and 2b illustrate an example of a circuit having a capacitance net to reduce cross-talk noise in accordance with one embodiment of the present invention.

[0018] Figure 3 illustrates a system for reducing cross-talk noise in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0019] The present invention includes a technique to reduce cross-talk noise that comprises increasing the non-coupling capacitance as a percentage of the total capacitance for a particular circuit design.

[0020] Figure 1 illustrates a flow diagram of a process for reducing cross-talk noise between a victim net and one or more aggressor nets in accordance with one embodiment of the present invention. It is noted that although the process is described with respect to a full chip analysis, the principles described herein may also work with a partial chip analysis, for example, by isolating a portion of the chip to be analyzed.

[0021] The process starts 110 with a full integrated circuit chip ("chip") analysis 115, which evaluates one or more chip performance characteristics, e.g., on chip noise or other measured voltage swings relating to noise characteristics, in view of the designed circuit layout. In one embodiment, the analysis provides a noise pulse height (or amplitude) for each net within the chip and the noise height may be stored in a database for reference against a predetermined noise margin (e.g., a maximum allowable noise height) for the chip as a whole, a portion of the chip, or the particular net. Further, in one embodiment the noise margin may be an amplitude value that is a predetermined percentage of the supply voltage value.

[0022] Next, the process identifies 120 those nets on the chip (or subset thereof) that have noise violations. Any of the one or more nets on the chip having noise violation would be the victim nets and neighboring nets around a victim net that cause or contribute to the noise violation of that victim net would be an aggressor net. Noise violations include noise pulses for a net that are above (or greater than) the predetermined noise margin.

[0023] The process selects 125 a victim net that has a noise violation for further analysis to determine a capacitance to add to reduce the noise on that victim net. For this, the process calculates 130 a change in ground capacitance of the victim net (ΔC_g) so that a noise amplitude (N_A) for the victim net is less than the maximum allowed noise height (or noise margin). In one embodiment, the analysis is carried out using equation:

$$N_A \cong (R_d C_c) / (R_d(C_g + C_c) + (Slew_{agg}/2)),$$

where N_A is a noise amplitude, R_d is a holding resistance of a victim net's driver, C_c is a coupling capacitance between a victim net and an aggressor net, C_g is a ground capacitance

of a victim net, and $Slew_{agg}$ is a slew of an aggressor net. From reviewing the above, it would be apparent to one of skill in the art, that increasing C_g will reduce the noise amplitude, N_A.

[0024] Once the change in ground capacitance is calculated, the process selects 135 from a library a cell having an input capacitance closest to (e.g., equal or just greater than or equal and just less than) the change in ground capacitance (ΔCg). In an alternative embodiment, if the largest input pin capacitance is unable to resolve the noise on the victim net, the process could add different sizes of library cells such that a total input pin capacitance of chosen library cells is equal to or greater than the required increase in ground capacitance and minimum number of library cells is used.

[0025] It is noted that a cell library includes a set of well-characterized logic blocks in an electronic design automation system. Further, it is noted that the cell may be a conventional logic element, for example, an inverter, or it may be a conventional capacitance cell from a cell library and that functions to provide circuit capacitance.

[0026] The process instantiates 140 the cell and places it close to the victim net in the circuit by connecting 145 the new cell input pin using conventional incremental routing techniques. It is noted that in one embodiment, placement of the cell is close to an input pin present on the victim net where a noise violation was worst, e.g., where the noise pulse height was highest or where the difference between the measured noise pulse height and the maximum allowable noise height (or noise margin) was greatest. Alternatively, the cell may be placed at any other location along the net such that the noise pulse height would drop below the allowable noise height (or noise margin) without affecting neighboring nets.

[0027] Once the cell is placed in the victim net, the process may conduct an optional incremental timing analysis 150 to evaluate timing between inputs and outputs, as well as between sequential elements on the chip. If the process determines 155 that the timing became worse, the changes will be rejected 160. If the process determines 155 that the timing has not become worse, the process will allow for acceptance of the changes. The process then determines 165 if there are more victim nets. If there are more victim nets, the process begins again by selecting 125 another victim net with a noise violation and working through the process as described above.

[0028] It is noted that the optional incremental timing analysis 150 could also include other optional tests separate from or in conjunction with this step. For example, the process may also analyze portions of the chip or a net for changes in slew and for total capacitance value on the net to determine if they are within predetermined allowable values in relation to the chip, portion of the chip, and/or the net. In addition, where appropriate, other chip characteristics may also be tested in view of the addition of the cell to the victim net, for example, electromigration and power consumption.

[0029] It is also noted that in one embodiment the process (or system) may be configured to set predetermined values (or parameters) for the particular test to be performed. Moreover, the process (or system) may also be configured such that a test value below or above the predetermined value for the particular test to be performed can be determinative of an adverse affect on the integrated circuit (or portion thereof).

[0030] Figures 2a and 2b illustrate an example of a circuit having a capacitance net to reduce cross-talk noise in accordance with one embodiment of the present invention. Figure

2a illustrates an initial circuit having an aggressor net that may include a first logic element 210 (e.g., a logic device, for example, an AND, OR, XOR, etc., or groupings thereof) and a second logic element 215 that are coupled through a coupling 217. The initial circuit illustrated also includes a victim net having a first logic element 220, a second logic element 223, and a third logic element 225, each coupled through coupling 227. In one embodiment, the couplings 217, 227 may be conventional wire couplings.

[0031] In this example, the layout of the circuit and the close coupling at a point A causes the noise pulse height of the victim net to be above a predetermined maximum allowable noise height for the circuit. Hence, using the process described herein and now shown in Figure 2, a cell 229 with a large input capacitance, e.g., C4, and coupled to the initial circuit so that the input pin, e.g., S3, of C4 couples an output pin of the first input element of the victim net, e.g., C1. This increases ground capacitance of the entire victim net so that the noise amplitude for the victim net is less than the maximum allowable noise height (or noise margin).

[0032] As a more particular example, consider C_g to be the total capacitance to ground, including the pin capacitances of pins S1, S2. In addition, consider the allowable noise amplitude on the victim net to be N_m (noise margin of the net). Then the noise slack (N_s) is given by the equation ($N_m - N_A$), so that for negative values of noise slack the net is said to be violating noise requirements. Further, an expression for ΔC_g can be obtained using the equation which yield to:

$$\Delta C_g = (-C_c * N_s) / (N_m * N_A)$$

From here, C4 may be chosen from the library as a cell that has at least ΔC_g or more input pin capacitance. It is also noted that in alternative embodiments, two or more cells from the library may be selected to achieve a capacitance value that is equivalent to a value for C4.

[0033] The present invention beneficially provides for a number of advantages and benefits. For example, the present invention does not disturb an overall solution for a circuit layout because it allows for reducing cross-talk noise between a victim net and one or more aggressor nets without adversely affecting other chip and/or net characteristics such as timings, slew, or overall capacitance.

[0034] In addition, the present invention advantageously touches a minimal number of wires, while guaranteeing convergence because new slews are always larger than previous slews. It is also noted that adding capacitance to a net without changing its driver size will increase slew on the net. In the case where this victim aggressing on another net, noise amplitude on the other net will also reduce. From reviewing the equation for N_A, it would be apparent to one of skill in the art, increasing $Slew_{agg}$ will reduce the noise amplitude, N_A on the other net.

[0035] It is noted that the present invention may be implemented in computer software, hardware, firmware, or a combination thereof. For example, the technique described herein may be embodied in modular functional components. Figure 3 illustrates an example system 305 for reducing cross-talk noise in accordance with one embodiment of the present invention. The system 305 includes a noise analyzer 310, a selector module 320, an analysis engine 330, a connection module 340, a cell library 350, and a test module 360. Each part of the system 305 may be configured to communicatively couple with each other.

[0036] The noise analyzer 310 is configured to perform chip noise analysis. For example, the noise analyzer 310 may be configured to test each net in the chip design and determine the noise level for each net. The selector module 320 is configured to identify and select those nets from the chip analysis that have noise violations. For example, the selector module 320 may be configured to include an allowable max noise height (or a threshold noise value) parameter that is used to identify and select nets with noise violations.

[0037] The analysis engine 330 is configured to perform analyses on each net. For example, the analysis engine 330 may be configured to perform a capacitance evaluation by calculating a change of C_g (ΔC_g) so that N_A is less than an allowable max noise height allowed (or threshold noise value) for each net. It is noted that the allowable maximum noise height value may be stored with the analysis engine 330 or could be stored elsewhere, e.g., the selector module 320. The analysis engine 330 may also be configured to perform other circuit analysis, for example, circuit timing analysis.

[0038] The cell library 350 is configured to store cells that may be placed (or connected) in the nets. For a particular net analyzed by the analysis engine 330, the connection module 340 is configured to select an appropriate cell (or group of cells) from the cell library 350 for that net based on the analysis engine 350 calculation of what ΔC_g should be to be less than (or equal to, depending on configuration and behavior sought for the net) N_A. The connection module 340 places (or connects) the selected cell (or group of cells) with that net using incremental routing. The test module 360 can then test the net with the added cell (or group of cells) to see if the noise level for the net is below the maximum allowed height. It is noted that in alternative embodiments the functionality of one or more components of the system 305 may be combined or collapsed into each other.

[0039] Upon reading this disclosure, those of skill in the art will appreciate still additional alternative structural and functional designs for a technique for reducing cross-talk noise between a victim net and one or more aggressor nets, in accordance with the disclosed principles of the present invention. Thus, while particular embodiments and applications of the present invention have been illustrated and described, it is to be understood that the invention is not limited to the precise construction and components disclosed herein and that various modifications, changes and variations which will be apparent to those skilled in the art may be made in the arrangement, operation and details of the method and apparatus of the present invention disclosed herein without departing from the spirit and scope of the invention as defined in the appended claims.